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Results:
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1 **Trace preconstruction**
Jacobson, Q.; Smith, J.E.
Computer Architecture, 2000. Proceedings of the 27th International Symposiu 2000
Page(s): 37 -46

[Abstract] [PDF Full-Text (912 KB)] **CNF**

2 **A dynamic multithreading processor**
Akkary, H.; Driscoll, M.A.
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE Inte Symposium on , 1998
Page(s): 226 -236

[Abstract] [PDF Full-Text (108 KB)] **CNF**

3 **A constraint logic programming algorithm for solving thermal unit commitment problem**
Hong-Tzer Yang; Kun-Yuan Huang; Ching-Lien Huang
Energy Management and Power Delivery, 1995. Proceedings of EMPD '95., 19 International Conference on , Volume: 1 , 1995
Page(s): 255 -260 vol.1

[Abstract] [PDF Full-Text (508 KB)] **CNF**

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DEPENDENC.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6
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DEPENDENCE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	138537
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DEPENDENCED.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
DEPENDENCEN.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
DEPENDENCEOF.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3
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L2	dispatch$3 near5 (before or after or previous$3 or recent$2) near5 (jump$3 or branch$3)	54	L2
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☐ 1. Document ID: US 6282633 B1

L35: Entry 1 of 21 File: USPT Aug 28, 2001

US-PAT-NO: 6282633
DOCUMENT-IDENTIFIER: US 6282633 B1

TITLE: High data density RISC processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6199152 B1

L35: Entry 2 of 21 File: USPT Mar 6, 2001

US-PAT-NO: 6199152
DOCUMENT-IDENTIFIER: US 6199152 B1

TITLE: Translated memory protection apparatus for an advanced microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 6031992 A

L35: Entry 3 of 21 File: USPT Feb 29, 2000

US-PAT-NO: 6031992
DOCUMENT-IDENTIFIER: US 6031992 A

TITLE: Combining hardware and software to provide an improved microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 6011908 A

L35: Entry 4 of 21 File: USPT Jan 4, 2000

US-PAT-NO: 6011908
DOCUMENT-IDENTIFIER: US 6011908 A

TITLE: Gated store buffer for an advanced microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw Desc | Image

☐ 5. Document ID: US 5958061 A

L35: Entry 5 of 21 File: USPT Sep 28, 1999

US-PAT-NO: 5958061
DOCUMENT-IDENTIFIER: US 5958061 A

TITLE: Host microprocessor with apparatus for temporarily holding target processor state

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw Desc | Image

☐ 6. Document ID: US 5926841 A

L35: Entry 6 of 21 File: USPT Jul 20, 1999

US-PAT-NO: 5926841
DOCUMENT-IDENTIFIER: US 5926841 A

TITLE: Segment descriptor cache for a processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
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☐ 7. Document ID: US 5926832 A

L35: Entry 7 of 21 File: USPT Jul 20, 1999

US-PAT-NO: 5926832
DOCUMENT-IDENTIFIER: US 5926832 A

TITLE: Method and apparatus for aliasing memory data in an advanced microprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 8. Document ID: US 5914727 A

L35: Entry 8 of 21 File: USPT Jun 22, 1999

US-PAT-NO: 5914727
DOCUMENT-IDENTIFIER: US 5914727 A

TITLE: Valid flag for disabling allocation of accelerated graphics port memory space

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 9. Document ID: US 5875464 A

L35: Entry 9 of 21 File: USPT Feb 23, 1999

US-PAT-NO: 5875464
DOCUMENT-IDENTIFIER: US 5875464 A

TITLE: Computer system with private and shared partitions in cache

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 10. Document ID: US 5860151 A

L35: Entry 10 of 21 File: USPT Jan 12, 1999

US-PAT-NO: 5860151
DOCUMENT-IDENTIFIER: US 5860151 A

TITLE: Data cache fast address calculation system and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 11. Document ID: US 5832205 A

L35: Entry 11 of 21 File: USPT Nov 3, 1998

US-PAT-NO: 5832205
DOCUMENT-IDENTIFIER: US 5832205 A

TITLE: Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 12. Document ID: US 5481685 A

L35: Entry 12 of 21 File: USPT Jan 2, 1996

US-PAT-NO: 5481685
DOCUMENT-IDENTIFIER: US 5481685 A

TITLE: RISC microprocessor architecture implementing fast trap and exception state

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 13. Document ID: US 5467459 A

L35: Entry 13 of 21 File: USPT Nov 14, 1995

US-PAT-NO: 5467459
DOCUMENT-IDENTIFIER: US 5467459 A

TITLE: Imaging and graphics processing system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 14. Document ID: US 5465361 A

L35: Entry 14 of 21 File: USPT Nov 7, 1995

US-PAT-NO: 5465361
DOCUMENT-IDENTIFIER: US 5465361 A

TITLE: Microcode linker/loader that generates microcode sequences for MRI sequencer by modifying previously generated microcode sequences

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 15. Document ID: US 5448705 A

L35: Entry 15 of 21 File: USPT Sep 5, 1995

US-PAT-NO: 5448705
DOCUMENT-IDENTIFIER: US 5448705 A

TITLE: RISC microprocessor architecture implementing fast trap and exception state

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 16. Document ID: US 5214753 A

L35: Entry 16 of 21 File: USPT May 25, 1993

US-PAT-NO: 5214753
DOCUMENT-IDENTIFIER: US 5214753 A

TITLE: Video system with parallel attribute interpolations

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 17. Document ID: US 5029070 A

L35: Entry 17 of 21 File: USPT Jul 2, 1991

US-PAT-NO: 5029070
DOCUMENT-IDENTIFIER: US 5029070 A

TITLE: Coherent cache structures and methods

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 18. Document ID: US 3858208 A

L35: Entry 18 of 21 File: USPT Dec 31, 1974

US-PAT-NO: 3858208
DOCUMENT-IDENTIFIER: US 3858208 A

TITLE: AUTOMATIC PRF SELECTION TO OPTIMIZE RANGE AND DOPPLER VISIBILITY IN RADAR TRACKING

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 19. Document ID: US 3858206 A

L35: Entry 19 of 21 File: USPT Dec 31, 1974

US-PAT-NO: 3858206
DOCUMENT-IDENTIFIER: US 3858206 A

TITLE: METHOD AND MEANS FOR OPERATING AN AIRBORNE SWITCHED ARRAY RADAR SYSTEM

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 20. Document ID: US 3833904 A

L35: Entry 20 of 21 File: USPT Sep 3, 1974

US-PAT-NO: 3833904
DOCUMENT-IDENTIFIER: US 3833904 A

TITLE: AIRBORNE SWITCHED ARRAY RADAR SYSTEM

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Term	Documents
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